UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ROBERT H. HAVEMANN

Appeal No. 2005-0287
Application No. 09/216,214

ON BRIEF

Before OWENS, KRATZ and POTEATE, Administrative Patent Judges.
KRATZ, Administrative Patent Judge.

## DECISION ON APPEAL

This appeal was taken pursuant to 35 U.S.C. § 134 from the refusal of the examiner to allow claims 8-10, 12, 14, 16, 18, 20, 22, 24, 26 and 27, which are all of the claims pending in this application.

## BACKGROUND

Appellant's invention relates to a transistor structure. An understanding of the invention can be derived from a reading of exemplary claims 9 and 10, which are reproduced below.

9. A transistor gate structure, comprising:

(a) a gate dielectric over a semiconductor region;

(b) a patterned gate over said gate dielectric having sidewalls, a top surface and a bottom surface disposed on said gate dielectric;

(c)a lateral growth on said gate dielectric at the corners of said gate, but not under central regions of said gate, the thickness of said gate dielectric continually increasing at the interface of said bottom surface and said sidewalls of said gate in a direction from said bottom surface toward and along said sidewalls; and

(d) a unitary electrically conductive metallic material entirely covering said sidewalls and top surface of said gate.

10. A transistor structure which comprises:

a region of semiconductor material having a gate dielectric thereover;

a polysilicon gate disposed over said gate dielectric having a top, a bottom and sidewalls;

a silicide layer disposed on said top and sidewalls of said polysilicon gate; and

source/drain regions in said region of semiconductor material spaced apart from each other, said source/drain regions each disposed adjacent to and aligned with said silicide layer disposed on said side

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

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| Watabe et al. (Watabe) | 4,727,038 | Feb. 23, 1988 |
| Arai | 5,841,174 | Nov. 24, 1998 |

Claim 10 stands rejected under 35 U.S.C. § 112, first paragraph as lacking written descriptive support in the application, as filed. Claims 8-10, 12, 14, 16, 18, 20, 22, 24, 26 and 27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Arai in view of Watabe.

We refer to the brief and reply briefs and to the answers for a complete exposition of the opposing viewpoints expressed by appellant and the examiner concerning the issues before us on this appeal.

OPINION

Upon careful review of the respective positions advanced by appellant and the examiner with respect to the rejections that are before us for review, we find ourselves in agreement with appellant's viewpoint in that the examiner has failed to carry the burden of establishing a prima facie case of lack of descriptive support. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1471-1472, 223 USPQ 785, 787-788 (Fed. Cir. 1984).

Accordingly, we will not sustain the examiner's § 112, first paragraph rejection on this record. However, our disposition of the examiner's obviousness rejection is another matter. In this regard, appellant has not persuaded us of any reversible error in the § 103(a) rejection before us. Thus, we shall affirm the examiner's § 103(a) rejection. Our reasoning follows.

The Rejection for Lack of Descriptive Support

Insofar as the written description requirement is concerned, "the PTO has the initial burden of presenting evidence or reasons why persons skilled in the art would not recognize in the disclosure a description of the invention defined by the claims." In re Wertheim, 541 F.2d 257, 263, 191 USPQ 90, 97 (CCPA 1976). "Precisely how close the original description must come to comply with the description requirement of § 112 must be determined on a case-by-case basis." Vas-Cath Inc. v. Mahurkar, 935 F.2d 1555, 1562, 19 USPQ2d 1111, 1116 (Fed. Cir. 1991). With regard to written descriptive support, all that is required is that appellant's specification reasonably conveys to one of ordinary skill in the art that as of the filing date of the application, appellant was in possession of the presently-claimed invention;

how the specification accomplishes this is not material. See In re Kaslow, 707 F.2d 1366, 1375, 217 USPQ 1089, 1096 (Fed. Cir. 1983); In re Edwards, 568 F.2d 1349, 1351-2, 196 USPQ 465, 467 (CCPA 1978).

The examiner has rejected claim 10 as not being described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. (answer, page 4).

The examiner has stated that descriptive support in the original disclosure could not be found because no support could be located in the original application disclosure for the claim 10 requirement that the source/drain regions are aligned with the silicide layer located on the polysilicon gate sidewalls (answer, pages 3 and 4). Concerning this matter, at page 8, lines 3-18 of the subject specification, appellant provides a detailed description as follows:

> Lightly-doped-drain extension regions (LDD regions 70) are then formed (step 130) by implantation of the exposed active area. This is followed by conformal deposition (step 140) of a metal 50, such as 20 nm of titanium, which will be used to form a silicide. This gives the structure shown in FIG. 2C. After deposition,

the source/drain areas receive their final doping, which is implanted (step 145) through the layer of metal to form regions 80. It is noted that the conformal metal on the sidewalls of the gate acts to mask that portion of the substrate from receiving this implant. An additional, optional implant (e.g., high-energy boron for an NMOS device) can be performed at this point (step 150), to form the HALO implant, if desired.

> The wafer is then annealed (step 155) to form a silicide on the gate and to disperse the dopants. Note that, since the source/drain areas are covered by an oxide, a silicide will not form in these regions. Unreacted metal will be stripped (step 160) from the gate area, giving the structure shown in FIG. 2D.

The examiner (answer, page 7) acknowledges that "according to Fig. 2C and page 8, lines 9-11 of the specification, it is true that source/drains 80 are formed aligned with the metal layer 50 before the formation of the metal silicide layer 60."

However, the examiner (answer, page 8) maintains that:

> a portion of the patterned polysilicon gate 20 and the metal layer 50 must be converted to the silicon layer 60. A careful observation of Fig. 2C and Fig. 2D clearly shows that the silicide layer 60 indeed encroaches and consumes a portion of the patterned gate 20 and the gate sidewalls have moved.

Based on the assertions of the examiner concerning alleged inward movement of the gate sidewall due to the silicide formation, and the further opinion of the examiner concerning alleged inward movement of the source/drain regions 80 under the gate because of dopant dispersal involved in appellant's

disclosed step 155, the examiner concludes that the source/drain regions would not be aligned with the silicide layer, as claimed. See answer, page 4.

Appellant, on the other hand, maintains that the originally filed application, particularly the first full paragraph of page 8 of the specification and drawing figures 2C and 2D make clear to one of ordinary skill in the art that appellant was in possession of the claimed subject matter because "the source/drain regions 80 are formed to the side of the sidewalls and are therefore in alignment with the silicide layer (which is merely the metal layer 50 converted to the silicide 60)." See pages 4 and 5 of the brief. As for the examiner's allegations of the movement of the gate sidewall boundary and the source/drain regions rendering the source/drain regions unaligned with the silicide layer, appellant maintains that "lateral dispersal of source/drain dopant is, at most, de minimus" (second reply brief, page 2) and appellant again notes the page 8 specification teaching that "conformal metal on the sidewalls of the gate acts to mask that portion of the substrate from receiving this implant" (second reply brief, page 3).

On this record, we side with appellant and do not agree with the examiner's alleged finding of a prima facie case of a lack of descriptive support for appealed claim 10. This is so because the examiner has not persuasively explained that a non-aligned arrangement of gate sidewall silicide and source/drain regions is taught by appellant's detailed description of the invention and supporting drawing figures wherein it is explained and shown that conformal gate sidewall metal, which metal is subsequently silicided, masks a portion of the substrate from receiving the dopant implant. Moreover, the masked portion of the substrate is adjacent to another substrate portion receiving the implant for forming source/drain regions of the substrate. While the examiner acknowledges that alignment is present before silicidation, the examiner proposes that the subsequently silicided metal will not be in alignment.

The examiner's supposition of non-alignment is principally based on alleged dopant migration and the silicidation reaction. However, that theory does not meet the examiner's burden of proving that alignment is not supported by the record before us.

In this regard, we further note that the claim term “aligned” is consonant with describing device features that are in proper relative position after using polysilicon gate structure in a self-aligning method as recited in appellant’s specification.[1]

Here, the examiner simply has not made the case as to why the so rejected claims would have been construed as describing possession of a new concept or invention not conveyed by the original disclosure for reasons set forth above and in the briefs. Consequently, on the present record, we find ourselves in agreement with appellant's basic position that the original disclosure reasonably conveys to the ordinarily skilled artisan that appellant had possession of the claimed subject matter, a position that the examiner has not effectively refuted by the rationale presented for the stated rejection. Therefore, the examiner’s rejection under § 112, first paragraph, with regard to the alleged lack of descriptive support cannot be sustained.

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[1] The term “aligned” as used in appellant’s claims does not require a strict linear or precisely parallel relationship of edges of the source drain regions and the gate sidewall silicide layer but rather is understood to encompass a proper relative positioning of those features within tolerances as would be understood by one of ordinary skill in the art. See, e.g., definitions 2 of “align” and definition 4a of “alignment” at page 53 of Webster's Third New International Dictionary, Meriam-Webster, Inc., Springfield, MA, 1993 (copy appended to decision).

§ 103 (a) Rejection

The examiner relies on the combined teachings of Arai and Watabe as evidence of obviousness in rejecting the claimed subject matter.[2]

We note that appellant (brief, page 3) maintains that the rejected claims do not stand or fall together for reasons set forth in the arguments. Accordingly, we consider the rejected claims separately to the extent that separate arguments have been presented in the briefs consistent with 37 CFR § 1.192 (c)(7) and (8), as in effect at the time of filing of the appeal briefs.

[2] In the supplemental answer (page 9), the examiner states that reliance on Tada (Japan Kokai 4-42938), a reference referred to in the obviousness rejection set forth in an earlier answer, has been withdrawn. Accordingly, we do not consider that reference as part of the evidence relied upon by the examiner in rejecting the appealed claims in the rejection before us. However, in the event of further prosecution of this subject matter before the examiner, the examiner and appellant should make of record a complete English language translation of Tada and the examiner should determine the patentability of the claims thereagainst.

Also, we are aware of appellant's concern regarding a perceived new ground of rejection. However, the record does not reflect that appellant sought any review of that perceived procedural transgression via the appropriate avenue of relief; that is, by way of petition to the appropriate examining supervisory authority.

Regarding appealed claims 8 and 9, appellant argues the claims together. Thus, we consider claim 9 as representative of claims 8 and 9.

Representative claim 9 requires a transistor gate structure including: (a) a semiconductor region with a gate dielectric thereon; (b) a patterned gate having top, bottom and side surfaces that is located on the gate dielectric; (c) an electrically conductive metallic material covering the gate sidewalls and top surface; wherein (d) the gate dielectric includes thicker portions (lateral growth) near sidewalls of the gate but not under central portions of the gate with the thickness of the dielectric increasing at the interfacing of the gate bottom surface and sidewalls in a direction from the bottom surface and toward and along the sidewalls.

As pointed out by the examiner in the supplemental answer (answer dated November 28, 2003, page 4), Arai discloses a transistor gate structure that includes “a gate dielectric 103 over a semiconductor region 101" and “a patterned gate 104(a) of polysilicon over said gate dielectric having sidewalls, a top surface and a bottom surface.” The examiner further takes the position that the bird’s beak construction of the dielectric that

is formed on the corners of the gate dielectric as shown in drawing figures 2B and 3A of Arai represents a thicker portion of

the dielectric that is located near the sidewalls of the gate but not under the central portion of the gate with the "thickness of the gate dielectric continually increasing at the interface of the bottom surface and sidewalls of the patterned gate in a direction from the bottom surface toward and along the sidewalls (Fig. 3A)" (supplemental answer, page 5). The examiner acknowledges that Arai does not explicitly employ an electrically conductive metallic material covering the gate sidewalls and top surface, as claimed by appellant. However, the examiner turns to Watabe[3] for teaching such a conductive layer (for example, titanium silicide). The examiner maintains that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the conventional feature (unitary electrically conductive metallic material of titanium silicide) onto the sidewalls and top surface of the patterned gate 104(a) of Arai in order to derive a portion of hot carriers through the gate electrode, and therefore the MOS transistor device whose transconductance is not degraded by hot carrier injection is obtained" (supplemental answer, page 5).

[3] Both Watabe and Arai are directed to metal-oxide-silicon (MOS) transistor devices.

Appellant acknowledges that Watabe discloses a silicided polysilicon gate structure. See second reply brief, page 3. However, appellant asserts that there is a lack of suggestion or teaching supporting the examiner's proposed combination of references. In this regard, appellant argues that because "Arai does not teach or even suggest a silicided polysilicon gate structure, any combination with Arai of a reference showing a silicided polysilicon gate could only be suggested by the subject disclosure and for no other reason" (second reply brief, page 3).

However, appellant's general assertion of a lack of combinability of the references does not specifically address the examiner's asserted rationale for modifying Arai based on the teachings of Watabe regarding the expectation of obtaining a transistor structure that would not be degraded by transconductance when employing such a conductive layer on the polysilicon gate. In this regard, we note that Watabe teaches that problems of increased resistance and degradation of transconductance due to hot carrier effects in a metal-oxide-silicon field effect transistor (MOSFET) can be prevented while using a conductive layer on the polysilicon gate and that the

device size can be minimized.[4] See, e.g., the abstract, column 1, lines 50-60, column 2, lines 3-8 and column 6, line 44 through column 7, line 24 of Watabe. That disclosure of Watabe is consistent with the examiner's stated rationale for combining the applied references, as referred to above. That rationale for the examiner's rejection has not been specifically refuted by appellant in the briefs before us in this appeal.[5]

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[4] Appellant appears to be concerned with the same problem. As set forth at the paragraph bridging pages 2 and 3 of appellant's specification:

> One of the long-standing problems in small field effect transistors is hot carrier effects. When a conventional MOS transistor structure is scaled down to one micron or less, the potential energy of an electron changes dramatically when it hits the N+ drain boundaries. This sudden change in potential energy in a short distance creates a high electric field. This is undesirable because it causes the electrons to behave differently within the semiconductor lattice. Electrons which have been activated by high electric fields are referred to as 'hot electrons', and can, for example, penetrate into or through the gate dielectric. Electrons which penetrate into, but not through, the gate dielectric can cause the gate dielectrics to become charged up over time. Thus, the behavior of the transistor will gradually shift in the field, until the transistor may fail in service. This is extremely undesirable.

[5] We note that arguments not made in the briefs are not generally considered by the Board. See 37 CFR 1.192(a), as in effect at the time the briefs were filed. That regulation has recently been replaced. See 37 CFR 41.37(c)(vii).

In addition, appellant submits that Arai does not teach or suggest to one of ordinary skill in the art, the option of employing a lateral growth at the corners of the gate dielectric but not under central gate areas such that the thickness of the dielectric increases in a direction from the bottom surface toward and along sidewalls of the gate.[6] As explained by the examiner, however, Arai does disclose such a gate dielectric thickening as depicted in drawing figure 3B and discussed in the disclosure of Arai as a bird's beak type structure. See, e.g., column 5, lines 37-45 of Arai.

It follows that on this record, we shall affirm the examiner's obviousness rejection of claims 8 and 9.

Concerning the other independent appealed claim, we note that claim 10 does not require a thickened dielectric layer at the gate corners. As for the recited silicide layer of claim 10, appellant acknowledges, as set forth above, that Watabe discloses

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[6] That argument is undercut by appellant's specification, wherein appellant acknowledges that "smiling oxidation," is a technique for forming a wider oxide thickness at the gate corners, which would have been commonly known. It is axiomatic that consideration of the prior art cited by the examiner must, of necessity, include consideration of the admitted state of the art found in appellant's specification. In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 687 (Fed. Cir. 1986); In re Davis, 305 F.2d 501, 503, 134 USPQ 256, 658 (CCPA 1962).

a silicided polysilicon gate structure. See the last line of page 3 of the second reply brief. As evidenced by a review of drawing figures 8A-8E and 9A-9E of Watabe and the corresponding text in the patent specification describing those drawing figures, Watabe teaches a transistor structure that includes: (a) a region of semiconductor material (1) that includes a gate dielectric (2) thereover; (b) a polysilicon gate (3) having a top, bottom and sidewalls as depicted in figures 8A-8E and 9A-9E; (c) a silicide layer (52 or 60) located on the top and sidewalls of the gate as depicted in drawing figures 8D, 8E, 9D and 9E; and spaced apart source/drain regions (5) adjacent to and aligned with the silicide sidewall layers as shown in drawing figures 8D, 8E, 9D and 9E. Thus, in addition to the reasons advanced above with respect to claim 9 and the reasons as stated in the answer with respect to the combined teachings of Watabe and Arai, Watabe alone reasonably suggests the claimed structure of appealed claim 10.

As for dependent claim 12, appellant argues the titanium silicide layer at page 8 of the brief. However, Watabe clearly describes siliciding titanium to form a layer of such a silicide over the gate at column 7, lines 13-18. Consequently, we do not find that additional argument persuasive.

Regarding dependent claims 14 and 16, appellant argues those claims together. Thus, we select claim 14 as representative of that claim grouping. With respect to representative claim 14 and the lightly doped source/drain extensions thereof, Watabe discloses such LDD structures as evident by a review of the patent disclosure and drawing figures 8D, 8E, 9D and 9E. Thus, in addition to the reasons set forth in the answer regarding the combined teachings of Watabe and Arai, Watabe alone reasonably suggests the structure of representative claim 14.

Concerning claim 26 and the requirement thereof that the silicide extend to a gate dielectric, as argued, we note that the sidewall silicide layers of drawing figures 8D, 8E, 9D and 9E of Watabe extend to the gate dielectric. Thus, in addition to the reasons set forth in the answer and above regarding the combined teachings of Watabe and Arai, Watabe alone reasonably suggests the argued structure of dependent claim 26.

Appellant groups claims 18, 20, 22 and 24 together at page 8 of the brief in arguing that the applied references do not teach or suggest a dielectric of increased thickness as claimed therein. We select claim 18 as a representative claim of that claim grouping. As explained above with respect to appealed claim 9 and for reasons stated in the answer, we do not find

appellant's arguments with respect to forming an increased dielectric thickness at the gate corners (a bird's beak or acknowledged conventional smiling oxidation formation) persuasive of a patentable distinction over the combined teachings of the applied references.

Having reconsidered the evidence of record for and against a conclusion of obviousness in light of the respective arguments advanced by appellant and the examiner, it is our determination that, on balance, the evidence weighs most heavily in favor of an obviousness conclusion with respect to the rejection under consideration.

It follows that we will affirm the examiner's § 103(a) rejection, on this record.

## CONCLUSION

The decision of the examiner to reject claim 10 under 35 U.S.C. § 112, first paragraph as lacking written descriptive support in the application, as filed is reversed. The decision of the examiner to reject claims 8-10, 12, 14, 16, 18, 20, 22, 24, 26 and 27 under 35 U.S.C. § 103(a) as being unpatentable over Arai in view of Watabe is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv).

AFFIRMED

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| TERRY J. OWENS<br>Administrative Patent Judge | ) |
| PETER F. KRATZ<br>Administrative Patent Judge | ) BOARD OF PATENT APPEALS AND INTERFERENCES |
| LINDA R. POTEATE<br>Administrative Patent Judge | ) |

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